CLAIMS

We claim:

1. A method of testing a combinational and sequential logic circuit with shift register latches of individual logic units coupled together to form a shift register scan path for testing logic circuits and uncoupled to disable the scan path while the logic circuit is performing its designed logic function, a method for reducing the heating of the circuit elements during testing comprising:

(a) dividing the circuits at least into two group cores;

(b) performing simulation testing by shifting a plurality of pseudo random pulse patterns through at least one of the cores to detect faults in said at least one of the cores;

(c) simultaneously performing simulation testing in other of said at least two cores using a weighted pseudo-random pulse pattern with the weighting selected to maintain the heating of the circuits below acceptable limits; and

(d) changing switching the cores subjected to the testing of the pseudo-random and the weighted pseudo-random test patterns so that pseudo-random and weighted pseudo-random test patterns are applied to all cores.

2. The method of claim 1, wherein said cores are on a single circuit chip.

3. The method of claim 2, wherein said circuit chip each of the cores contain the circuits of the core connected for self testing to a pseudo-random pattern generator and data compression means capable of providing the pseudo-random and the weighted pseudo-random patterns separately to each core.

4. The method of claim 3, wherein there are a plurality of circuit chips capable of self testing and on a single module.

5. The method of claim 4 the module is tested by subjecting at least one of the circuit chips to the pseudo-random self test patterns while others of the chips are subjected to the weighted pseudo-random pattern.

6. The method of claim 1, wherein each of the cores is a chip on a module.

7. A computer program on a computer useable medium for testing a combinational and sequential logic circuit with shift register latches of individual logic units coupled together to form a shift register scan path for testing logic circuits and uncoupled to disable the scan path while the logic circuit is performing its designed logic function, a method for reducing the heating of the circuit elements during testing comprising:

(a) software for dividing the circuits at least into two group cores;

(b) software for performing simulation testing by shifting a plurality of pseudo random pulse patterns through at least one of the cores to detect faults in said at least one of the cores;

(c) software for simultaneously performing simulation testing in other of said at least two cores using a weighted pseudo-random pulse pattern with the weighting selected to maintain the heating of the circuits below acceptable limits; and

(d) software for changing switching the cores subjected to the testing of the pseudo-random and the weighted pseudo-random test patterns so that pseudo-random and weighted pseudo-random test patterns are applied to all cores.

8. The computer program of claim 7, wherein said cores are on a single circuit chip.

9. The computer program of claim 8, wherein said circuit chip each of the cores contain the circuits of the core connected for self testing to a pseudo-random pattern generator and data compression means capable of providing the pseudo-random and the weighted pseudo-random patterns separately to each core.

10. The computer program of claim 9, wherein there are a plurality of circuit chips capable of self testing and on a single module.

11. The computer program of claim 10, wherein the module is tested by subjecting at least one of the circuit chips to the pseudo-random self test patterns while others of the chips are subjected to the weighted pseudo-random pattern.

12. The computer program of claim 11, wherein each of the cores is a chip on a module.